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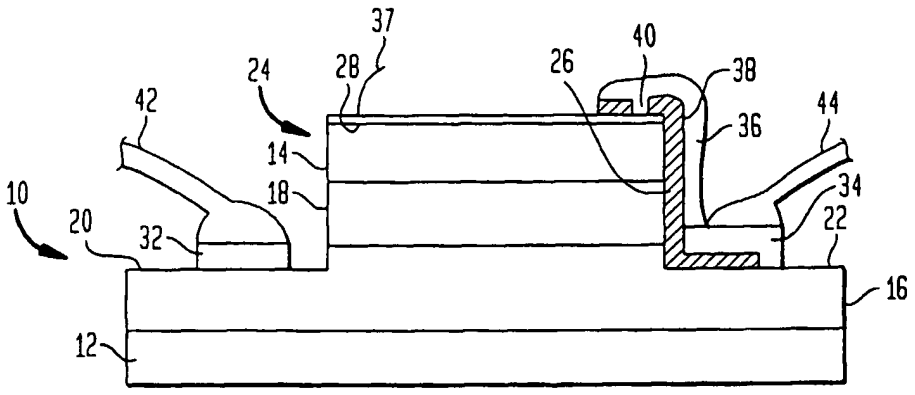
(54) Title: LED LEAD FOR IMPROVED LIGHT EXTRACTION



(57) Abstract: Light emitting diodes (LEDs) are provided with electrode and pad structures, wich result in improved light extraction for the LED. The LED may be foremd as a die withan upper contact surface (28) and a lower contact surface (20,22). A mesa (24) including at least one generally vertical edge surface (26) projects upwardly from the lower contact surface. First and second pads (32, 34) are disposed on teh lower contact surface. The second pad desirably does not make ohmic contact with the lower contact surface. A conductive lead (36) is in bridging contact with the second pad and the upper contact surface of the mesa.

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LED LEAD FOR IMPROVED LIGHT EXTRACTION

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims benefit of United States Provisional Patent Application 60/273,591, the disclosure of which is incorporated by reference herein.

TECHNICAL FIELD

The present invention relates to optoelectronic devices such as light-emitting diodes.

BACKGROUND ART

Light emitting diodes or "LEDs" include thin layers of semiconductor material of two opposite conductivity types, referred to as p-type and n-type. The layers are disposed in a stack, one above the other, with one or more layers of n-type material in one part of the stack and one or more layers of p-type material at the other end of the stack. For example, the various layers may be deposited in sequence on a substrate to form a wafer. The wafer is then cut apart to form individual dies, which constitute separate LEDs. The junction between the p-type and n-type material may include directly abutting p-type and n-type layers, or may include one or more intermediate layers which may be of any conductivity type or which may have no distinct conductivity type. In operation, electric current passing through the diode is carried principally by electrons in the n-type layers and by electron vacancies or "holes" in the p-type layers. The electrons and holes move in opposite directions toward the junction and recombine with one another at the junction. Energy released by electron-hole recombination is emitted as light. As used in this disclosure, the term "light" includes radiation in the infrared and ultraviolet wavelength ranges, as well as radiation in the visible range. The wavelength of the light depends on factors

including the composition of the semiconductor materials and the structure of the junction.

Electrodes are typically connected to the n-type and p-type layers near the top and bottom of the stack. The materials in the electrodes are selected to provide low-resistance interfaces with the semiconductor materials. The electrodes, in turn, are provided with pads suitable for connection to wires or other conductors, which carry current from external sources. The pad associated with each electrode may be a part of the electrode, having the same composition and thickness of the electrode, or may be a distinct structure, which differs in thickness, composition, or both from the electrode itself.

Some LEDs have electrodes on the bottom surface of the bottom semiconductor layer. For example, the various layers may be deposited in sequence on an electrically conductive substrate, and the substrate may be left in place on the bottom surface to act as a bottom electrode. Thus, LED's formed from AlInGaP typically use conductive GaAs substrates and may have an electrical connection to the substrate. However, LEDs formed from certain semiconductor materials normally use nonconductive substrates to promote proper formation of the semiconductor layers. The nonconductive substrate typically is left in place, so that an electrode cannot be provided on the bottom surface of the bottom layer. For example, gallium nitride-based materials such as GaN, AlGaN, InGaN and AlInGaN are used to form LEDs emitting light in various wavelength ranges including blue and ultraviolet. These materials typically are grown on insulating substrates such as sapphire.

LEDs incorporating an insulating substrate must include a bottom electrode at a location on the stack above the substrate but below the junction. Typically,

the upper layer or layers of the stack are removed after formation of the stack in a region covering part of the area of each die, so as to provide an upwardly-facing lower electrode surface on a layer at or near the bottom of the stack in each die. This leaves a region referred to as a "mesa" projecting upwardly from the lower electrode surface and covering the remaining area of the die. The area of the die occupied by the lower electrode surface does not emit light. It is typically desirable to keep the horizontal extent of this inactive area as small as possible.

The top electrode typically includes a pad formed on the top surface of the stack, i.e., the top surface of the top semiconductor layer, and the pad makes ohmic contact with this top layer. Typically, the layers in the stack above the junction are transparent, so that light emitted at the junction can pass out of the stack through the top surface. The top electrode and pad are arranged so that they do not block all of the emitted light. It is desirable for the opaque top electrode and pad to cover only a small portion of the top surface of each die. However, the current passing from such an electrode will tend to flow downwardly through the stack so that the current passes predominantly through the area of the junction disposed beneath the electrode. This phenomenon, referred to as "current crowding," results in light emission concentrated in that area of the junction beneath the electrode, where it will be blocked by the electrode and pad. The amount of useful light reaching the outside of the die per unit of electrical current passing through the die, commonly stated as the external quantum efficiency of the die, is reduced by this phenomenon. Current crowding is a significant consideration with LEDs formed from

materials having relatively high electrical resistivity, such as the gallium nitride-based materials.

The minimum size of the top pad is limited by solder ball bonding technology to approximately 100 microns in width or diameter. The typical width or diameter of the top surface of a mesa is approximately 300 microns. The relatively large size of the bonding pad with respect to the top surface of the mesa negatively impacts the light extraction efficiency of the LED device due to reflections from absorption in the bonding pad metal. Therefore, there is a need to improve the problem of reduced light extraction beneath the pad.

DISCLOSURE OF THE INVENTION

The present invention addresses these needs.

One aspect of the invention provides a light-emitting diode including a stacked structure. The stacked structure incorporates a first region of a first conductivity type, a second region of a second conductivity type and a light-emitting p-n junction between these regions. The stacked structure defines a lower contact surface and a mesa projecting upwardly from the lower contact surface. The mesa includes at least one generally vertical edge surface. The first type region is disposed in the mesa and includes an upper contact surface.

The light emitting diode according to this aspect of the invention includes a first pad in contact with a first portion of the lower contact surface and electrically connected to the stacked structure through the lower contact surface. A second pad is in contact with a second portion of the lower contact surface. Preferably, the second paid is electrically isolated from the stacked structure at the lower contact surface. A conductive lead extends between the second pad and the

upper contact surface. The conductive lead preferably overlies a portion of the mesa, including the generally vertical edge surface thereof. The lead is preferably electrically connected to the first-type region through the upper contact surface.

According to one aspect of the invention, the region of the second conductivity type defines the lower contact surface. Preferably, the conductive lead overlies only a portion of the upper contact surface. In another aspect of the invention, a dielectric layer is sandwiched between the conductive lead and the portion of the mesa covered by the conductive lead. In this aspect, the dielectric layer extends between the second pad and the lower contact surface. According to this aspect of the invention, preferably the dielectric layer overlies a portion of the upper contact surface and there is an opening through a portion of the dielectric layer overlying the upper contact surface to expose the upper contact surface. The opening allows the conductive lead to make ohmic contact with the upper contact surface. In a preferred aspect, a transparent electrode overlies and is in ohmic contact with the upper contact surface, the lead is connected to the transparent electrode at the opening.

According to a highly preferred aspect of the invention, the opening through the dielectric layer is generally circular in cross section and has a diameter of less than about 20 microns, more preferably less than about 10 microns. In another preferred aspect of the invention, the opening is located adjacent the edge surface of the mesa. As noted above, a typical LED configuration involves placement of an electrode-pad unit on the upper contact surface of the mesa. The relatively large size of the pad reflects and absorbs

light generated in the LED device, which decreases the light extraction efficiency of the device.

According to the present invention, the conductive lead which establishes ohmic contact through the dielectric layer covers a much smaller area than pads which are typically arranged on the top of the mesa. Such a design substantially reduces the amount of material blocking light generated from the LED and will reduce the reflection and absorption losses. Thus, the present invention provides a light emitting diode that has improved light extraction.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a front elevational view of an LED in accordance with one embodiment of the invention.

Fig. 2 is a view similar to FIG. 1 but depicting an LED in accordance with a further embodiment of the invention.

MODES FOR CARRYING OUT THE INVENTION

Figure 1 shows an LED in accordance with one embodiment of the invention. The LED includes a stacked structure of semiconductor layers 10 on a substrate 12. The stacked structure includes semiconductor material of a first conductivity type in a first or upper region 14 of the stack and material of a second, opposite conductivity type in a second or lower region 16 adjacent substrate 12. For example, the first or upper region 14 may be formed from a p-type semiconductor whereas the second or lower region 16 may be formed from an n-type semiconductor. The semiconductors may be III-V semiconductors, for example, GaN materials. The term "gallium nitride based semiconductor" as used herein refers to a nitride based semiconductor including gallium. However, the present invention is not limited to a particular type of semiconductor. Other semiconductor materials, including other III-V materials

are within the scope of this invention. The p-type and n-type conductivity may be imparted by conventional dopants and may also result from the inherent conductivity type of the particular semiconductor material.

The stacked structure 10 includes a junction 18 between the first and second regions. The junction is symbolized in Fig. 1 as a discrete layer interposed between regions 14 and 16. In practice, the first and second regions may abut one another so that they define the junction at their mutual border. Alternatively, the junction may include additional layer structures in the mutually adjacent portions of regions 14 and 16 or between these regions. For example, regions 14 and 16 may include clad layers adjacent junction 18. The clad layers typically have greater band gap than the material constituting the junction. Thus, the junction may be a simple homojunction; a single heterojunction, a double heterojunction, a multiple quantum well or any other type of junction structure.

Also, each of regions 14 and 16 can include any number of layers. Merely by way of example, the second or lower region may incorporate a "buffer layer" at the interface with substrate 12. Alternatively, a diffusion layer may be included in the first region to allow current to diffuse into the LED structure. The diffusion layer should be of the same conductivity type as the remainder of the first region 14. The diffusion layer may incorporate a highly doped contact layer at the top of the stack to aid in establishing ohmic contact with a conductive lead.

According to the present invention, the upper layer or layers of the stack, including the first region 14, the junction 18 and a portion of the second region 16, are removed after formation of the stack to provide

upwardly-facing lower electrode surfaces 20 and 22 on a layer at or near the bottom of the stack in each die. This leaves a mesa 24 projecting upwardly from the lower electrode surface and covering the remaining area of the die. The area of the die occupied by the lower electrode surface does not emit light. The mesa 24 includes at least one generally vertical edge surface 26 and an upper contact surface 28.

The fabrication processes used to form the stacked structure are well known. Most commonly, the various layers which form the stacked structure are deposited on the substrate in sequence by techniques such as metal organic chemical vapor deposition ("MOCVD") molecular beam epitaxy and the like.

A first pad 32 is provided on a first portion 20 of the lower contact surface. The first pad is electrically connected to the lower contact surface. That is, the first pad is connected to the lower contact surface such that current can pass between the first pad and the material of the second-type region defining the lower contact surface. Most preferably, the first pad 32 itself is in ohmic contact with the lower contact surface. Preferably, the first pad 32 includes a metal that will form ohmic contact with lower contact surface 20. Examples of such metals include gold (Au) and nickel (Ni). Alternatively, the first pad 32 may be formed from a metal which does not make ohmic contact with the second-type semiconductor material defining the lower contact surface, and an electrode layer (not shown) formed from a metal which does make ohmic contact with the lower contact surface is interposed between the first pad 32 and the lower contact surface.

A second pad 34 overlies a portion of the lower contact surface 20 , this portion being indicated at 22 in the drawings. Portion 22 most typically is coplanar

with the other portions of lower contact surface 20, but this is not essential. Preferably, the second pad is electrically isolated from the second-type semiconductor material defining the lower contact surface. That is, the second pad is arranged so that there is no substantial current flow between the second pad and the semiconductor material at the lower contact surface during normal operation of the device. In the preferred embodiment illustrated, a dielectric layer 38, further discussed below, extends between the second pad 36 and the lower contact surface 22.

A conductive lead 36 is in bridging contact with the second pad and the upper contact surface 28 of the mesa 24. That is, the conductive lead is electrically connected to the second pad and to the upper contact surface. Preferably, the conductive lead 36 overlies at least a portion of the second pad 34, the generally vertical edge surface 26 of the mesa adjacent the second pad, and a portion of the upper contact surface 26 of the mesa 24. The conductive lead 36 may include a metal that can form an ohmic contact directly with the upper contact surface, such as gold or nickel. Alternatively, a transparent electrode 37 (as shown in FIG. 2) directly overlies the upper contact surface and lead 36 is connected to the electrode so that the lead is connected to the upper contact surface by way of the transparent electrode.

Referring back to FIG. 1, in a preferred aspect of the invention, a dielectric layer 38 is sandwiched between the conductive lead 36 and the portions of the mesa 24 covered by the conductive lead 36. The dielectric layer 38 prevents ohmic contact between the second pad 34 and the lower contact surface and prevents the p-n junction 18 from being shorted by the bridging conductive lead 36. Examples of suitable dielectric

materials for the dielectric layer include SiO_x, SiN_x, Al_2O_3, TiO_2, and combinations thereof.

According to another aspect of the invention, an opening 40 is provided through a portion of the dielectric layer overlying the upper contact surface 28. Preferably, this opening is generally circular in cross section and has a diameter less than about 20 microns, more preferably, less than about 10 microns. In another aspect of the invention, the opening in the dielectric layer is preferably located adjacent the generally vertical edge surface of the mesa. As shown in Figure 1, the opening 40 through the dielectric layer allows the conductive lead 36 to establish ohmic contact with the upper contact surface 28 of the mesa. It is desirable to keep the size of the opening and the area of conductive lead as small as possible while still ensuring ohmic contact with the upper contact surface. The opening is formed through the dielectric layer using standard photolithographic and etching processes known in the art. The conductive lead and opening desirably covers an area that is less than about 20 microns in width or diameter, which is significantly smaller than the conventional pads that are typically 100 microns in diameter.

In an alternative arrangement, the opening in the dielectric layer is omitted, and an end of the lead extends beyond the dielectric layer and overlies the top contact surface. This end makes electrical contact with the top contact surface, or with an electrode on the top contact surface. For example, the dielectric layer may terminate at the edge of the top contact surface. In another alternate arrangement, the second pad 34 can be formed integrally with conductive lead 36, so that a portion of the conductive lead constitutes the second pad.

In a further alternative arrangement, all or a part of the dielectric layer 26 may be omitted. For example, where the material of the second pad 34 is selected so that it does not make ohmic contact with the material of lower region 16, the barrier provided by the non-ohmic contact as, for example, a Schottky diode formed by the second pad and the material of the lower contact region at surface 22, may prevent current flow between the second pad and the lower region. In this case, the dielectric layer 26 need not extend between the second pad and the lower contact surface. Thus, pad 34 may directly abut lower contact surface portion 22. Similarly, where a barrier is formed between the material of lead 36 and the material of the edge surface, the dielectric layer on the edge surface can be omitted. Also, the dielectric layer can be omitted in those cases where some current flow from the pad or lead into the semiconductor layers can be tolerated. For example, current flow from lead 36 into the upper layer 14 can be tolerated, and the dielectric layer can be omitted at those portions of the edge surface bounding the upper layer 14.

In the embodiments discussed above, the lower contact surface portions 20 and 22, and both portions of the lower contact surface are defined by the lower region 16. In a variant, the portion 22 of the lower contact surface bearing the second pad may be defined by the substrate. Thus, the material of the lower region 16 may be etched away in this area. If the substrate is dielectric, no dielectric layer need be provided between the second pad and this portion of the lower contact surface.

Conversely, the dielectric layer 26 can be extended over other regions of the semiconductor structure so that the dielectric layer serves as a passivation layer

and protects the structure from physical damage or contamination. For example, the dielectric layer may cover the upper contact surface 28 (Fig. 1) or the transparent conductive electrode 37 (Fig. 2). In this case, the dielectric layer desirably is transparent.

Pads 32 and 34 are connected to leads 42 and 44 which in turn are connected to an external circuit (not shown) for actuating the LED. Desirably, pads 32 and 34 are large enough to accommodate wire bonding or other conventional bonding processes used to connect the leads to the pads. For example, the pads may have diameters on the order of 75-150 microns, most typically about 90-125 microns. Because both pads are disposed on the lower contact surface, and away from the upper contact surface 28, the pads do not occupy any portion of the upper contact surface and do not block light passing out of the structure through the upper contact surface 28 or through transparent electrode 37. Although some portion of the upper contact surface or electrode surface is occupied by the end of lead 36, this portion can be considerably smaller than the area of the second pad. Thus, the preferred embodiments of the invention minimize the area of opaque structures on top of the mesa, and allow a greater proportion of the light generated within the structure to exit through the top of the die. Stated another way, by avoiding the need for a second pad on top of the die, preferred embodiments of the present invention enhance the external quantum efficiency of the die.

It should be appreciated that the figures are not drawn to scale. In particular, the thicknesses of the various layers have been greatly exaggerated for clarity of illustration. Typically, the entire stack is on the order of five microns thick. The horizontal dimensions of the die, such as the overall die width W and die

length L are on the order of a few hundred microns as, for example, about 200-700 microns. The die is typically rectangular or, most preferably, square with equal width and length. Although the preferred embodiments have been described above with reference to particular semiconductor materials, it will be appreciated that the invention can be applied with dies formed from other semiconductor materials as well. Also, the conductivity types can be reversed, so that in some cases the first or upper region can be formed from n-type semiconductor material whereas the second or lower region may be formed from p-type semiconductor materials.

As these and other variations and combinations of the features discussed above can be utilized without departing from the present invention, the foregoing description of the preferred embodiments should be taken by way of illustration rather than by way of limitation of the invention as defined by the claims.

CLAIMS:

1. A light-emitting diode comprising:

(a) a stacked structure including a first region of a first conductivity type and a second region of a second conductivity type and a light-emitting p-n junction between said regions, said stacked structure defining a lower contact surface and a mesa projecting upwardly from said lower contact surface, said mesa including at least one generally vertical edge surface, said first-type region being disposed in mesa and including an upper contact surface;

(b) a first pad overlying a first portion of the lower contact surface and electrically connected to the stacked structure through said lower contact surface;

(c) a second pad overlying a second portion of the lower contact surface but electrically isolated from the stacked structure at said lower contact surface; and

(d) a conductive lead extending between the second pad and the upper contact surface, the conductive lead overlying a portion of the mesa including the edge surface thereof, the lead being electrically connected to the first-type region through said upper contact surface.

2. The light-emitting diode of claim 1, wherein said region of said second conductivity type defines the lower contact surface.

3. The light-emitting diode of claim 1 wherein said first pad makes ohmic contact with said region of said second conductivity type at said lower contact surface.

4. The light-emitting diode of claim 1, further comprising a dielectric layer extending between said second pad and said lower contact surface, whereby

said dielectric layer electrically isolates said second pad from said lower contact surface.

5. The light-emitting diode of claim 1, wherein the conductive lead overlies only a portion of the upper contact surface.

6. The light-emitting diode of claim 5, wherein said portion of the upper contact surface is of lesser area than said second pad.

7. The light-emitting diode of claim 5, further including a dielectric layer disposed between the conductive lead and said portion of the mesa.

8. The light-emitting diode of claim 7, wherein said dielectric layer extends between the second pad and the lower contact surface.

9. The light emitting diode of claim 7, wherein said dielectric layer overlies a portion of the upper contact surface, the dielectric layer further including an opening through a portion of the dielectric layer overlying the upper contact surface, the lead being electrically connected to the upper contact surface through said opening.

10. The light emitting diode of claim 8, further comprising a transparent electrode overlying said upper contact surface and in ohmic contact therewith, said lead being connected to said transparent electrode at said opening.

11. The light-emitting diode of claim 8, wherein said mesa is generally in the form of a rectilinear solid and said top surface of said mesa is generally rectangular.

12. The light-emitting diode of claim 11, wherein said opening is generally circular in cross section and has a diameter of less than about 20 microns.

13. The light-emitting diode of claim 12, wherein said opening is located adjacent said edge surface of said mesa.

14. The light-emitting diode of claim 12, wherein said first conductivity type is p-type and said second conductivity type is n-type.

FIG. 1

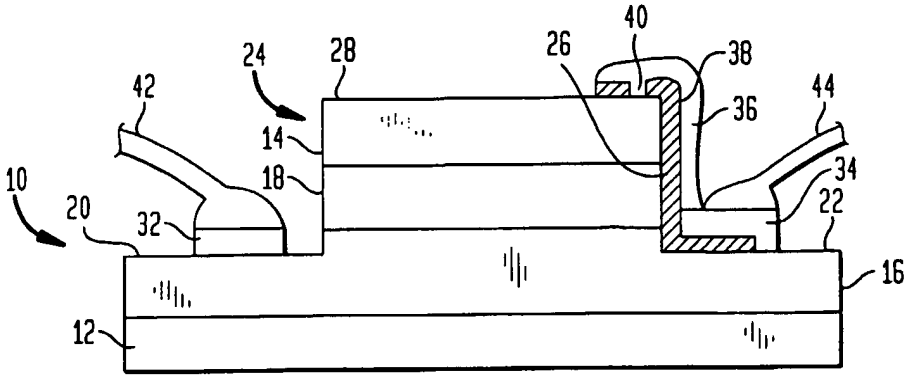
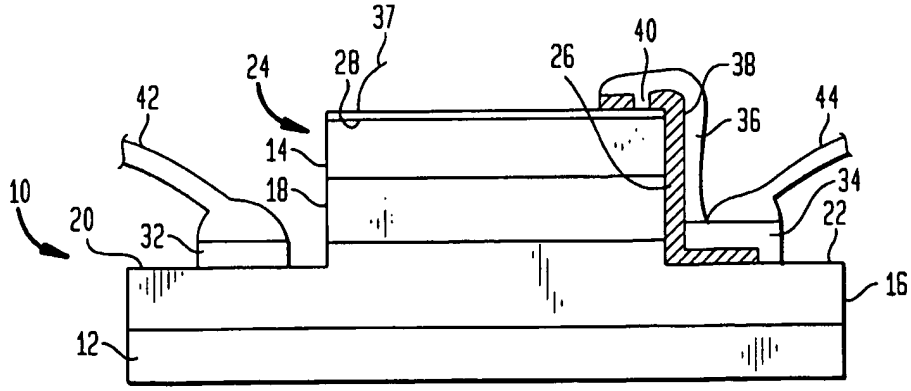


FIG. 2



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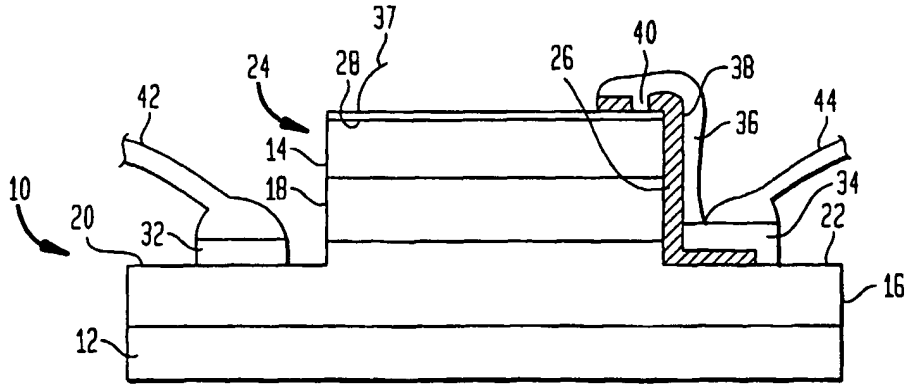

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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US CL : 257/91, 99, 744, 745
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/91, 99, 744, 745

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A, P	US 6,281,524 B1 (YAMAMOTO et al.) 28 August 2001 (28.08.2001), see entire document.	1-14
A	US 6,130,446 A (TAKEUCHI et al.) 10 October 2000 (10.10.2000), see entire document.	1-14

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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